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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,638	03/30/2001	Ryou Nakagaki	16869P023300	6928

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EXAMINER	
SHAPIRO, JEFFERY A	

ART UNIT	PAPER NUMBER
3653	

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,638	NAKAGAKI ET AL.	
	Examiner	Art Unit	
	Jeffrey A. Shapiro	3653	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,23-28 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,23-28 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5, 6, 8, 9, 27 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dor et al (US 6,744,266 B2) in view of Stephan et al (US 6,338,001 B1) , further in view of Nishimura et al (US 5,761,337), further in view of Kumagai (US 5,394,481), further in view of Jarvis et al US 6,297,644 B1).

Dor et al discloses the following.

As described in Claims 1, 6 and 9;

a. imaging an inspected semiconductor wafer object (204, 206) (see col. 5, lines 10-16);

b. extracting an image (1208, 1210 and 1212) of a defect candidate from an image obtained by said imaging step;

c. classifying said extracted defect candidate image into a first category (see figure 14, noting defects are classed into the various types illustrated);

As further described in Claim 9;

d. said second category relating to predicted yield from said inspected object (316);

e. said first category in a map format (see col. 6, lines 35-42.)

Dor further discloses as described in Claims 7, 10 and 23-25, the imager is a scanning electron microscope (206).

Further regarding Claims 1, 6 and 9, Dor et al discloses as follows:

f. displaying on a screen said extracted defect candidate image *together with first and second classification information, said first classification information relating to* said first category, *said second classification information relating to* said second category;

g. *said step of classifying said extracted defect candidate image into said second category is performed by comparing a circuit pattern area and a defect area, said circuit pattern area being obtained from a reference image and said defect area being obtained from said imaging step*;

See Dor et al, figures 4, 5,12 and 14. Figure 4 illustrates an internet browser having various defect images (442) that can be opened up into another browser, as described in col. 14, lines 59-61, classes (432), denoted A-C, for example, and causes of said defects. See also col. 11, lines 53-66. Figure 12 includes case ID, case name, and images (1208, 1210 and 1212) displayed near each other under the tab "case".

Another tab is noted as "classification". Figure 14 illustrates the classes tab displaying the various classes that defects are classified under. Note also figure 9, which illustrates defect detail including images and graphs of data.

Dor does not expressly disclose the use of kill ratio data as a comparison criteria for displaying along with defect image and classification data, for example. However, Stephan discloses using kill ratio data (112, 310) in analyzing semiconductor wafer defects.

At the time of the invention, it would have been obvious for one ordinarily skilled in the art to have included kill ratio data in Dor's display screens.

The suggestion/motivation would have been because one ordinarily skilled in the art would have recognized based upon Dor's disclosure, as described above, that effective review and comparison of the chip defects would be enhanced by use of kill ratio data, as taught by Stephan. See Stephan, col. 1, line 59-col. 2, line 10, col. 4, lines 65-67 and col. 5, lines 1-10.

Dor discloses the system described above. Dor does not expressly disclose, but Nishimura et al, Kumagai and Jarvis disclose the following;

As described in Claims 1, 5, 6, 8, 9, 27 and 33;

h. said defect type includes one or more of the following: particle defects, flaw defects, circuit pattern short defects, circuit pattern open defects and voltage contrast defects;

As described in Claims 1, 5, 9 and 33;

i. calculating third information relating to voltage contrast of the defect candidate;

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have inspected a wafer for particle defects, flaw defects, circuit pattern short defects, circuit pattern open defects and voltage contrast defects as described in Claims 1, 5, 6, 8, 9, 27 and 33.

The suggestion/motivation would have been to obtain defect information on semiconductor wafer defects. See Dor, abstract.

Note that figure 9 of Kumagai discloses various types of defects charted, such as holes, spots and breaks that fall into the categories of particle defects, flaw defects. Kumagai also discloses breaks, which can be construed as circuit pattern open defects, as described in section "h" above. Figure 3 of Nishimura discloses images of various connection faults and short circuits, said short circuits and connection faults construed as voltage contrast defects, as described in section "h and i" above. Note that an inspection system such as that of Dor et al determines such defects, as one ordinarily skilled in the art would recognize them as well-known semiconductor circuit defects found in wafers during manufacturing.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have calculated third information related to voltage contrast defects as described in Claims 1, 5, 9 and 33.

The suggestion/motivation would have been to obtain defect information on semiconductor wafer defects. See Dor, abstract.

Regarding Claims 1, 5, 9 and 33, note that Jarvis discloses and teaches actual testing equipment and techniques regarding detection of voltage contrast flaws by flowing electrons through the circuits and obtaining voltage readings for comparison with expected voltages. See Jarvis et al (US 6,297,644), last four lines of abstract and figures 9a, 9b, 10a, 10b and 11, illustrating short circuit situations and col. 2, lines 66 and 67, col. 3, lines 1-9, and col. 7, lines 58-col. 8, line14, mentioning use of a scanning electron microscope (SEM) to perform such voltage contrast studies of defects. Therefore, based on Jarvis' teaching, it would have been obvious for one ordinarily skilled in the art to have used Dor's SEM to obtain voltage contrast information and then to have calculated third information data relating to said voltage contrast for a particular wafer.

Priority

3. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Response to Arguments

4. Applicant's arguments filed 9/11/06 have been fully considered but they are not persuasive. Applicant asserts that Dor can not be used as prior art because Dor's earliest priority date of 10/2/00 is before Applicants' date of 5/18/00. However, this date relied upon by Applicants is obtained from Japanese foreign Application JP00-152663, the original document of which has been filed in the application in the Japanese language. Therefore, the rejection of Applicants' claims over Dor, Stephan, Kumagai, Nishimura and Jarvis is maintained.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dudasko '474, Pinto '439, Takagi '965, Queisser '953, Yoda '347, '472, '507, '601 and '808, Takagi '194, '308 and '965, Koshishiba '998, Nakagaki '705, Ishikawa '893, chen '459, Zika '596, Tobin '776, Eskridge '381, Shimoda '081 and Saidin '294 are all cited as examples of semiconductor wafer inspection systems.

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey A. Shapiro whose telephone number is (571)272-6943. The examiner can normally be reached on Monday-Friday, 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick H. Mackey can be reached on (571)272-6916. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAS

November 28, 2006

PATRICK MACKEY
SUPERVISORY PATENT EXAMINER
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